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Non-Volatile and Gate-Controlled Multistate Photovoltaic Response in WSe_2/h-BN/Graphene Semi-Floating Gate Field-Effect Transistors

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Semi-floating gate field-effect transistors (SFG-FETs) based on 2D materials have received much attention due to their unique optoelectronic characteristics, potential applications in near-memory computing and constructing sensing-memory-processing units. Here, the non-volatile and gate-controlled multistate photovoltaic response of a WSe_2/h-BN/graphene SFG-FET is investigated both in experimental and theoretical aspects. Due to the ambipolar carrier transport of WSe_2 channel, both electrons and holes can be stored in the graphene floating gate layer, which results in two evident memory windows on the round sweep transfer characteristic curve. Different charge-stored states of the SFG layer enable the channel to form a lateral junction that can be adjusted by the gate voltage, which leads to the gate-controlled multistate photovoltaic response. A theoretical model is implemented to explain the memory and the multistate photovoltaic response behaviors in a quasi-quantitative level. The relationship between the charge-stored states in the SFG and the photo-response, as well as its dependence on the gate voltage are systematically analyzed. These research results provide a reliable way for realizing high-performance multi-functional photodetectors based on SFG-FETs and for thorough understanding the complicated optoelectronic behaviors of SFG-FETs.

1. Introduction

Floating gate (FG) field-effect transistors (FETs) based on 2D materials are an important candidate for constructing sensing-memory-processing and logic-in-memory devices,[1–5] which have many potential applications.[6–19] Semi-floating gate (SFG) introduces an extra interesting feature of forming a gate-controllable lateral pn junction in the channel of SFG-FET.[20–25] Semiconductor pn junctions are fundamental building blocks for optoelectronic devices, for example, light-emitting diodes, solar cells, and photodetectors. Due to the low carrier density of states of 2D materials, the major charge type and the carrier density can be tuned by an electrostatic field, enabling the formation of tunable pn junctions.[26–28] In the work of Hu et al., van der Waals (vdW) heterodiodes with unilateral depletion region demonstrate a record high power conversion efficiency and a fast response time, which lays a foundation for the next generation of vdW heterostructure photovoltaic devices.[29] In 2021, Hu and Ye et al. pioneered a novel brain-inspired neuromorphic hardware with a unique homogeneous transistor-memory architecture, experimentally performing a disruptive sensing-memory-computing integrated application in artificial intelligence realm, which has become a milestone to guide the development of brain-inspired intelligence and the revolutionary non-von Neumann computing system.[3] The

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combination of non-volatile memory and tunable lateral pn junction in a SFG-FET creates various possibilities for realizing novel optoelectronic devices, for example, the integrated sensing-memory-processing units for edge computing in internet of things.[3–5,13,16–19]

The memory-state-dependent pn junctions in SFG-FETs have various interesting properties. Li et al.[20] have realized a WSe_2 SFG-FET that can be operated as a non-volatile memory. Different homogeneous junction states can be configured in the WSe_2 channel by changing the type and density of stored carriers in the SFG layer. The formation of pn junction in the channel evidently enhances the programming/erasing current ratio. The logic optoelectronic functions have been demonstrated in a $MoTe_2$ SFG-FET.[21] Such optoelectronic logics originate from the photovoltaic response of the lateral $MoTe_2$ pn junction that can be reconfigured by the density and polarity of the stored carriers in the SFG.[21] Zhou et al.[23] have shown that in a SFG-FET, the photoelectric response can be used to simulate the perception of human visual system. Recently, in a graphene/h-BN/WSe_2 SFG-FET, various synaptic functions have been emulated with the device gated by triboelectric potential.[24] Using the SFG infrastructure, it is possible to enhance the detection performance of various photodetectors based on 2D materials.[30–33]

Carrier transfer between the SFG layer and the channel in a SFG-FET is a key clue to understand the complicated optoelectronic behaviors of SFG-FETs. By measuring the electrostatic potential of FG layer, Sasaki et al.[34] proposed a model that during the round sweep of back-gate voltage, the transfer characteristics are determined by the capacitive coupling and the feedback tunneling between the FG and the channel, and the large hysteresis on the round-sweep transfer curves is well explained in a qualitative level. However, the lateral junction states along the channel and their dependence on the carrier storage in the FG layer were not experimentally explored and not included in their model. In this paper, the non-volatile and gate-dependent multistate photovoltaic response of a WSe_2/h-BN/graphene SFG-FET was systematically investigated both in experimental and theoretical aspects. There are two evident memory windows in the round-sweep transfer curve corresponding to the hole and electron storage states in the SFG layer. Under the 520 nm laser illumination, the device shows complicated gate-dependent multistate photovoltaic response behaviors, from which the built-in electrical field and lateral junction configurations can be elucidated. A phenomenological model is established (Section S1, Supporting Information) to analyze the photovoltaic response and its dependence on the carrier storage state in the SFG layer. The numerical results are in good agreement with the experimental data. Our research does not only provide a way to realize integrated sensing-memory-processing devices, but also establish a method to deeply understand the complicated optoelectronic behaviors of SFG-FETs.

2. Results and Discussion

Figure 1a shows the schematic of the SFG-FET. A multilayer van der Waals semiconductor WSe_2 is selected as the channel. The ambipolar transport property of WSe_2 promises the formation of all the lateral junction configurations along the channel. A hexagonal-BN (h-BN) layer is underneath the channel, acting as the tunneling barrier. Between the p^+-Si/SiO_2 (the SiO_2 layer is 280 nm thick) substrate and the h-BN tunneling barrier, there is a multilayer graphene FG layer. Only part of the WSe_2 channel at the drain terminal (Left) is vertically overlapped with the graphene SFG layer, and the residual component of the channel at the source terminal (Right) cannot be gated by the SFG, which results in the nonuniform SFG-induced doping and the formation of a lateral junction. The device was prepared by combining the standard mechanical exfoliation method and the polydimethylsiloxane (PDMS) assisted dry transfer method. Then e-beam lithography was employed to define the electrodes, and thermal evaporation and lift-off processes were used to form the Pt/Au (15 nm/80 nm) electrodes. The detailed fabrication processes are presented in Figure S2 (Supporting Information). Finally, the device was annealed for 120 min at 473 °C in Ar atmosphere to remove the adsorbed impurities on the surface and improve the device stability. The atomic force microscope measurements show that the thicknesses of the multilayer WSe_2, h-BN, and graphene are 90, 10, and 30 nm, respectively. A thick WSe_2 channel was selected to improve the photovoltaic response and to prevent the influence of photon-assisted tunneling across the h-BN layer. The illuminated light with photon energy larger than the bandgap of WSe_2 (≈1.3 eV)[35] will be completely absorbed by the 90 nm-thick WSe_2 channel, which is beneficial for enhancing the photo-response and avoiding the unexpected influences of the penetrated photons on carrier tunneling across the h-BN barrier.[36] Since the density of states of graphene is approximately proportional to the layer numbers, the Fermi level change is smaller for storing the same amount of carriers for a thicker SFG graphene layer (30 nm) and a deeper trapping potential will be formed to improve the charge retention ability. The optical microscopy image of the WSe_2/h-BN/graphene SFG-FET is shown in Figure 1b. As shown in Figure 1c, typical Raman signatures of WSe_2 (E_{2g} peak at 247 cm^{-1} and A_{1g} peak at 254 cm^{-1}),[37] h-BN (E_{2g} peak at 1366 cm^{-1}),[38] and graphene (G peak at 1581 cm^{-1} and 2D peak at 2723 cm^{-1})[39] are clearly observed in the corresponding Raman spectra, indicating good performance of the mechanically exfoliated materials. The source-drain current-voltage (I_{ds}-V_{ds} with drain voltage sweeping from −0.5 to 0.5 V) curve (Figure 1d) at zero back-gate voltage (V_{BG}) was performed to characterize the metal-WSe_2 contacts. The antisymmetric I_{ds}-V_{ds} curve with respect to (0, 0) point indicates that there is no built-in electrical field along the WSe_2 channel. The weak non-linear relation of I_{ds}-V_{ds} in the voltage range of −0.25–0.25 V originates from small Schottky barriers located at the source and drain metal-WSe_2 contacts.[40] Such small Schottky barriers have no remarkable influences on the memory and optoelectronic properties of the SFG-FET.

Electrical measurements were performed to character the memory properties of the SFG-FET. **Figure 2a** presents the transfer curve of the SFG-FET with a round-sweep of V_{BG} from −40 V (V_{start}) to 40 V (V_{turn}) and vise verse at a sweep speed of 0.2 V s^{-1}, the SFG in the floating state, and a constant drain-source voltage of 0.1 V. Such a slow sweep speed of V_{BG} promises that the drain-source current I_{ds} reaches its steady value at each point of V_{BG}. Further measurements show that the round-sweep transfer curve is unchanged with a sweep speed <0.3 V s^{-1} (Figure S3, Supporting Information). As shown in Figure 2a, different from the

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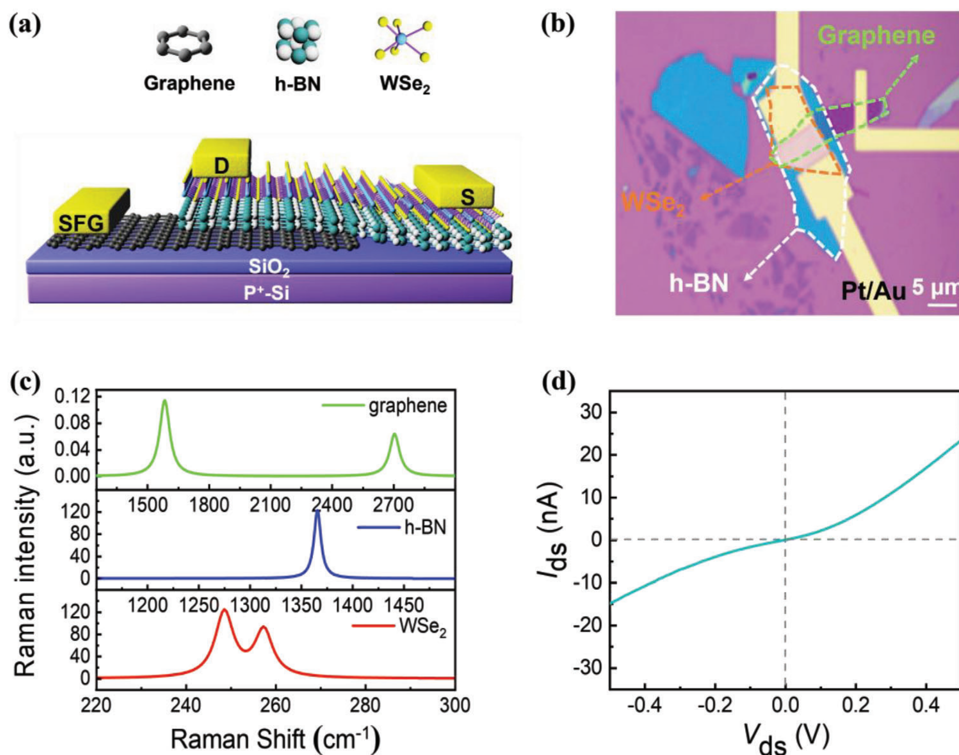

Figure 1. The structure and basic electrical properties of the WSe_2/h-BN/graphene SFG-FET. a) Schematics of the WSe_2/h-BN/Graphene SFG-FET. b) Optical microscopy image of the mechanically-exfoliated SFG-FET with the WSe_2, h-BN, and graphene marked by orange, white, and cyan dotted lines, respectively. c) Raman spectra of WSe_2, h-BN, and graphene, respectively. d) Output I_{ds}-V_{ds} curve with zero back-gate voltage and the SFG in the floating-gate state.

reported measurements for the similar device structures,[20,34,41] there are two clear memory windows on the round-sweep transfer curve due to the carrier tunneling across the h-BN layer and excess electrons (holes) trapped on the graphene SFG layer. The device shows a good retention time (Figure S4a, Supporting Information). The falling edges of the two memory windows (at V_{BG} = −40 and 35 V for the left and right windows, respectively) are much steeper than the corresponding rising edges (at V_{BG} = −30 and −15 V). Especially at V_{BG} = −40 V, a small decrease of the negative V_{BG} will induce a giant reduction of I_{ds} by about three orders of magnitude, which is a charming feature for constructing switches and amplifiers.[9] The on/off ratio of the memory windows are limited by the small bias voltage of V_{ds} = 0.1 V and the bias-dependent resistance of the Schottky Au-WSe_2 contacts. The round-sweep transfer curves were measured for $V_{start} = -V_0$ and $V_{turn} = V_0$ with V_0 increasing from 10 to 50 V at a step of 10 V (Figure S3, Supporting Information). For the cases of V_0 = 10 and 20 V, only the right memory window appears, and with V_0>30 V, the left memory window begins to appear. Due to the sharp falling edge of the left memory window, there is a random shift of the falling edge with different values of V_0. For FG-FETs, the relationship of stored excess carrier concentration in the FG layer and the width of the memory window is $n_{2D} = \Delta V_{BG} C_{h-BN}$. As shown in Figure S3 (Supporting Information), the width of the right wider memory window is a linear function of V_0. The time-dependent memory behaviors are briefly presented in Figure S4 (Supporting Information).

To further understand the round-sweep transfer characteristic curve shown in Figure 2a, the V_{BG} -dependent carrier concentrations (Figure 2b) and the Fermi energies (Figure 2c) of the left and right components of WSe_2 channel are numerically calculated, and then the built-in voltage as a function of V_{BG} (Figure 2d) is derived. The detailed computational procedure [42,43] and the fitting parameters are presented in Section S1 (Supporting Information). The turbostratic stacking is approximated for the floating gate multilayer graphene, and the density of states is proportional to the layer number of graphene (Equation S4 in Supporting Information). According to the variation tendency of current, the round-sweep transfer characteristic curve can be divided into seven sections labeled by numbers 1–7. In section 1-2, the hole concentrations of the two channel components decrease, which results in the sharp reduction of drain current. In section 2-3, a constant current of 10^{-10} A is maintained with V_{BG} in the range of −37 to −18 V. As shown in Figure 2b, at the beginning of section 2-3, the hole concentration approaches to zero, and then the major carrier becomes electron, thus the left channel is in high-resistance state and the transport behavior is dominated by the left component of channel. Sequentially, the same process occurs in the right component of the channel, which leads to the low constant current in section 2-3. With the forward sweep of V_{BG} from −18 to −9 V, the major carrier is electron in the whole channel; the electron concentrations and consequently the drain current increases in section 3-4. In section 4-5, as shown in Figure 2b, the electron concentration

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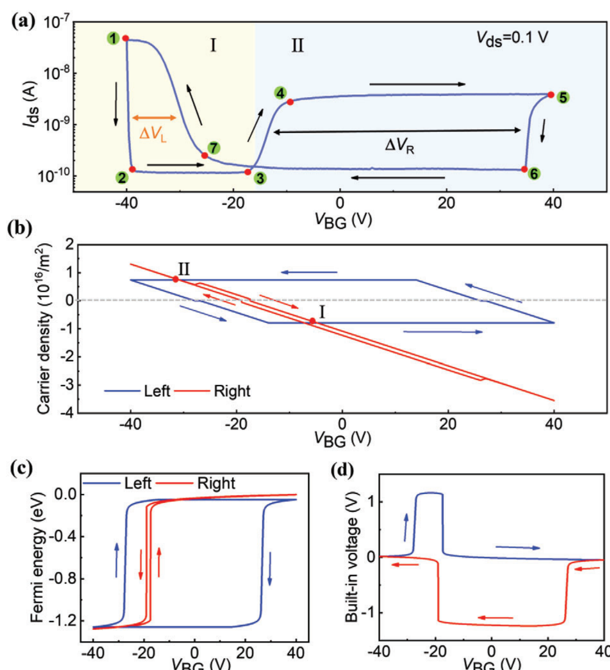

Figure 2. Electrical characteristics of memory behavior and numerical results of V_{BG}-induced doping in the WSe_2 channel of the SFG-FET. a) Round-sweep transfer characteristic curve with the V_{BG} from V_{start} = −40 V to V_{turn} = 40 V and a fixed V_{ds} of 0.1 V. Due to the different types of stored carriers in the SFG layer, there are two clear memory windows (the yellow I and blue II regions for the left and right ones, respectively) on the round-sweep transfer curve. The sweep rate of V_{BG} is 0.2 V s^{-1}, and the value is fixed in the following experiments if not specified. b) Numerical results of carrier concentrations. c) Fermi energies. d) Built-in voltage of the left and right side of WSe_2 channel as functions of round-sweep gate voltage.

in the left component of the channel increases slightly with V_{BG} ranging from −9 to 2 V and then keeps constant with V_{BG} sweeping from 2 to 40 V; in the right component of the channel, the electron concentration increases monotonously with respect to V_{BG}. In this section, it seems that the current is limited by the left component of the channel, which nearly keeps constant in a wide range of V_{BG}. For the backward sweep V_{BG} ranging from 40 to −20 V, the drain current is dominated by the left component of the channel, in which the electron concentration decreases sharply and approaches to zero in section 5-6. Due to the low electron concentration near zero in the right component of the channel, the drain current nearly remains constant in section 6-7. The increase of drain current in section 7-1 is due to the increase of hole concentration in the right component of the channel. The obvious magnitude difference of drain current near point 1 and in section 4-5, cannot be caught by our model, which maybe due to the difference of hole and electron mobility.

The Fermi energies of both sides of WSe_2 channel with respect to round-sweep V_{BG} (Figure 2c) can be derived from the corresponding carrier concentrations (Figure 2b). The band bending and the built-in voltage are directly linked to the difference of Fermi energies of the left and right sides of the channel. Due to the influence of stored carriers in the SFG layer, the calculated rising and falling edges of Fermi energy of the left side of channel locate at V_{BG} of ≈−30 and 10 V for forward and backward sweeps, respectively. On the contrary, the rising and falling edges (corresponding to the conversion point of major carrier types) of Fermi energy are nearly overlapped for the right side of the channel. The slight difference of V_{BG} at which the rising and falling edges are located originates from the influence of the left side of the channel. Figure 2b,c indicate that all the junction configurations can be formed between the left and right sides of WSe_2 channel. The large built-in voltages (positive and negative in the V_{BG} ranging from −30 to −18 V and 25 to −20 V for forward and backward sweeps, respectively), as shown in Figure 2d, are due to the formations of np and pn junctions. However, the different junction configurations do not introduce remarkable features in the round-sweep transfer characteristic curve (Figure 2a). The possible reasons maybe the long channel length, the small depletion region,[44] and the small source-drain bias voltage.

The memory windows presented in Figure 2a originate from two different coupling states, the capacitive coupling and feedback tunneling,[35,42] between the SFG layer and the WSe_2 channel. In the capacitive coupling state, because the electrical field is lower than the Fowler–Nordheim (FN) tunneling threshold field, carriers cannot directly tunnel across the h-BN barrier,[45,46] and the carrier concentration in the SFG layer is unchanged. However, in the feedback tunneling state, carrier exchange occurs between the SFG layer and the WSe_2 channel through FN tunneling across the h-BN barrier. In this process, if the sweep velocity of V_{BG} is slow enough to reach a steady state, due to the screening effect of excess carriers, the electrostatic potential of the SFG layer will be pinned to a fixed value, the FN tunneling threshold electrical field, which has been identified experimentally.[35,42] In an ideal condition, the FN tunneling threshold electrical field is determined by the Fermi energies of SFG layer and WSe_2 channel and the thickness of h-BN barrier. In our computational model, we assume that if the Fermi energy of the graphene SFG or the WSe_2 channel aligns with the conduction (valence) band edge of h-BN at the opposite side of the barrier, electron (hole) FN tunneling is triggered (The assumption will have some influences on the electrical properties of the SFG-FET in some detailed aspects, but has no essential influences on our main conclusion).

The simulated electrostatic potential and carrier concentration of SFG layer as functions of round-sweep V_{BG} are shown in **Figure 3**a,b, respectively. The memory window in the round-sweep transfer characteristic curve originates from the different dependences of floating gate potentials and carrier concentrations in the SFG layer on the forward and backward sweep of V_{BG}. Figure 3c presents the band alignment of SFG layer, h-BN barrier, and WSe_2 channel at zero back gate voltage and with no excess carriers in the SFG layer and the WSe_2 channel. The energy differences between the Dirac point of SFG and the bottom (top) of conduction (valence) band of h-BN barrier is 2.05 eV (3.85 eV).[36] Therefore, if the Fermi energy is not far away from the Dirac point, only electron tunneling from the SFG layer to the WSe_2 channel is considered. Based on the same reason, the carrier in the reverse tunneling is also electron. The band alignments for different values of V_{BG} are presented in Figure 3d–f, from which the capacitive coupling and the feedback tunneling states can be clearly identified. At V_{start} = −40 V, the FN tunneling is triggered. Due to the screen effect of excess carriers in the SFG layer, the electrical field across the h-BN barrier will return

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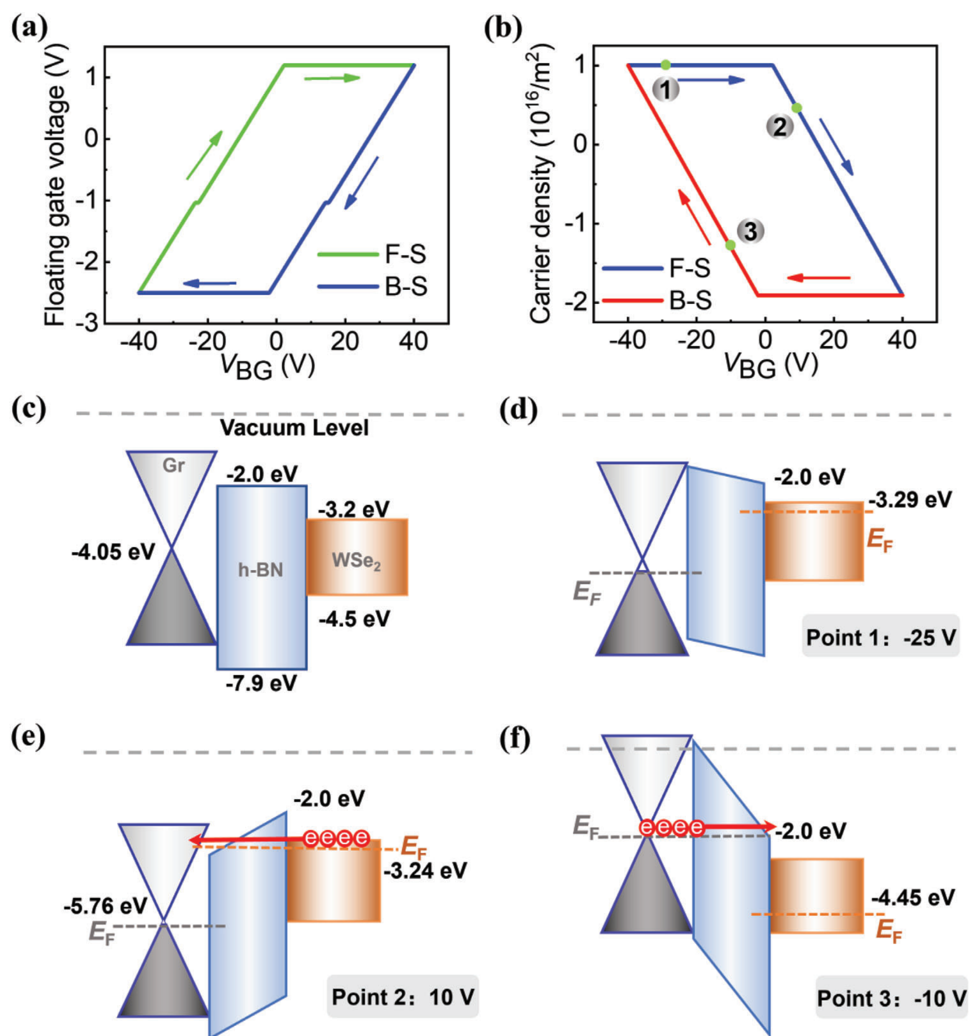

Figure 3. Numerical results of electrostatic potential voltage of the SFG layer a) and carrier concentration b) in the SFG layer with respect to round-sweep of V_{BG}. c) Band alignments of SFG, h-BN, and WSe_2 at $V_{BG} = 0$ V and with no excess carriers in the SFG layer and WSe_2 channel. Numerical results of band alignments for d) $V_{BG} = -25$ V (Point 1 in b), capacitive coupling), e) 10 V (Point 2 in b), feedback tunneling coupling), and f) −10 V (Point 3 in b), feedback tunneling coupling). F-S: forward sweep; B-S: backward sweep.

to the threshold electrical field value and the FN tunneling is terminated, and the system reaches to a steady state. For the forward (backward) sweep of V_{BG} from −40 to −1 V (40 to 0 V), as shown in Figure 3a,b, the electrostatic potential of the SFG linearly increases (decreases) with V_{BG} and the carrier concentration in the SFG layer keeps constant, which means the system is in the capacitive coupling state. The numerical calculated band alignment for the capacitive coupling state at the forward sweep $V_{BG} = -25$ V (Point 1 in Figure 3b) is shown in Figure 3d. The Fermi energy of the SFG (WSe_2 channel) is lower (higher) than the conduction (valence) band edge of h-BN at the opposite side of tunneling barrier, according to our assumption, electrons and holes cannot pass through the h-BN barrier via FN tunneling. For the forward (backward) sweep range of V_{BG} from −10 to 40 V (0 to −40 V), the floating gate voltage is pinned to 1.0 V (−2.5 V), which is the fitted value of p_{VT} (n_{VT})[35] described in Section S1 (Supporting Information), and the carrier concentration in the SFG layer linearly decreases (increases) with the value of V_{BG}. In these two regions of V_{BG}, the SFG-FET is in the feedback tunneling state. The band alignments at forward (backward) sweep $V_{BG} = 10$ V (−10 V), the point labeled as 2 (3) in Figure 3b, is depicted in Figure 3e,f. For the case of Point 2, the Fermi energy of the SFG layer aligns with the conduction band edge at the opposite side of barrier, then the electrons will tunnel across the h-BN barrier from the SFG layer to the WSe_2 channel. However, for the case of Point 3, the Fermi energy of WSe_2 channel aligns with the conduction band edge at the opposite side of barrier, the electron tunneling direction is reverse. Hole tunneling across h-BN barrier in similar device structures has been reported.[45,46] Based on the band alignment data,[36] electron tunneling across the h-BN barrier is adopted in this work. In fact, in our investigations, the hole tunneling is equivalent to the inverse electron tunneling. Therefore, further investigations are needed to identify this point.

Photovoltaic response is not only an important optoelectronic property of SFG-FET, but also directly linked to the built-in

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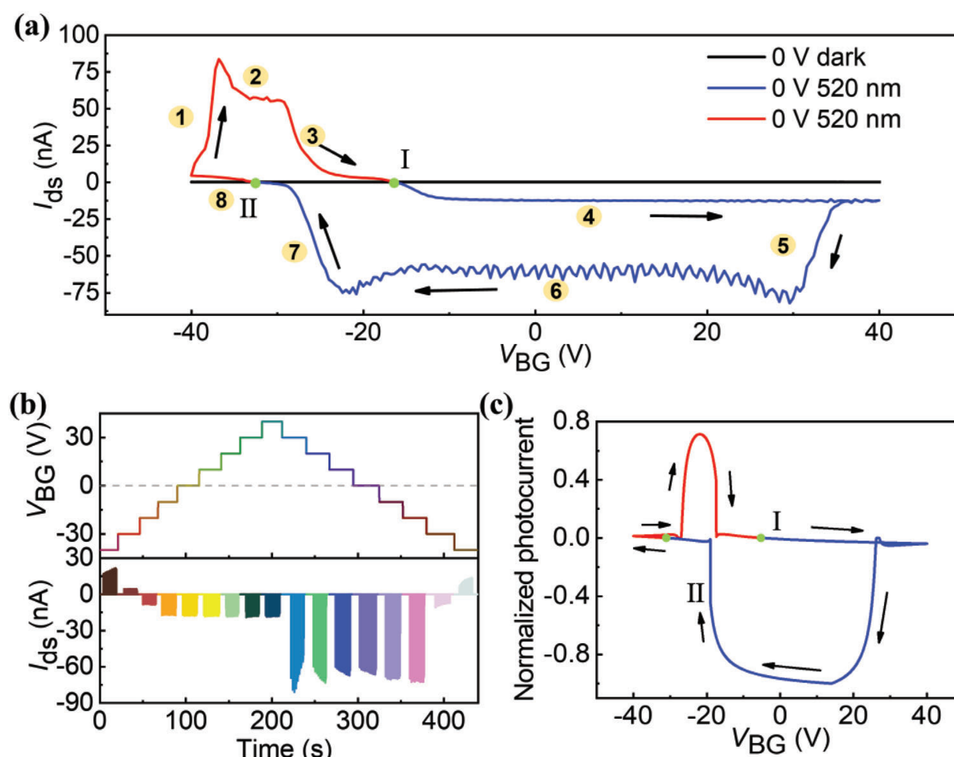

Figure 4. Round-sweep gate-dependent multistate photovoltaic response (short-circuit current) of the SFG-FET. a) Round-sweep zero-bias source-drain currents (I_{ds}) in the conditions of dark and 520-nm laser illumination with V_{BG} sweeping from −40 to 40 V and vice verse. b) Zero-bias photocurrent pulses under the stepped round sweep of V_{BG} from −40 to 40 V. c) Numerical results of round-sweep zero-bias photocurrent with V_{BG} sweeping from −40 to 40 V.

voltage of the lateral junction formed in the channel of SFG-FET. **Figure 4** shows the multistate zero-bias photovoltaic response under the illumination of a 520 nm laser with respect to the round sweep of V_{BG} from −40 to 40 V. In comparison with the round-sweep transfer characteristic curve (Figure 2a), some extra subtle features can be revealed from the zero-bias short-circuit photocurrent with respect to the round-sweep of V_{BG}. The photocurrent curve is composed of eight segments, corresponding to different lateral junction configurations in the WSe_2 channel. In segment one, the SFG-FET is in the capacitive coupling state; in the left component of channel, the hole concentration decreases to zero, and then the major carrier type changes from hole to electron, which leads to the junction configuration changing from pp^+ to np (Figure 2b) and the resultant sharply rising of built-in voltage (Figure 2d) and photocurrent. In segment two, the np junction configuration continues and the hole concentration in the right side of channel decreases with V_{BG}, resulting in the slightly reduction of photocurrent. In segment three, the major carrier becomes electron in the whole WSe_2 channel and the channel is in the n^+n configuration; in this region, there is a conversion of the capacitive coupling state to the feedback tunneling state. The zero photocurrent point I corresponds to the intersection Point 1 in Figure 2b. In segment four, the channel is in the nn^+ configuration and there is a small and negative photocurrent. At the beginning of segment five, the nn^+ configuration continues, and then the major carrier in the left component of channel becomes hole, which results in the formation of pn junction, large reverse built-in voltage, and strong negative zero-bias photocurrent. In segment six, the pn configuration continues; the fluctuation of photocurrent is due to the mechanical/electrical interruption noise. In segment seven, the major carrier of the right component of channel becomes hole, the channel junction configuration changes from pn to p^+p, and then both the built-in voltage and photocurrent decrease. The second zero photocurrent Point II corresponds to the intersection point 2 in Figure 2b. Finally, in segment eight, the channel is in a pp^+ configuration, resulting in a small position zero-bias photocurrent. The other detection performance parameters of the SFG-FET are shown in Figures S5–S7 (Supporting Information). According to the simulation results, the schematics of all the junction configurations are depicted in Figure S8 (Supporting Information).

The time-dependent photovoltaic response with a round step sweep V_{BG} is shown in Figure 4b. There is a fast response time of zero-bias photocurrent to the step sweep V_{BG}. The magnitude and polarity of photocurrent pulses are in agreement with the data shown in Figure 4a. The numerical photovoltaic response is calculated using Equation S6 (Supporting Information) and the result is shown in Figure 4c. A resistance R_0 (Equation S6, Supporting Information) is introduced as a fitting parameter to describe the resistance of the junction depletion region and the other parasitic resistances. Compared to the experimental data shown in Figure 4a, the main features of zero-bias photocurrent are reproduced, which indicates that our theoretical model describes the dynamic processes in SFG-FETs well. The differences

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between the numerical results and experimental data shown in Figure 4a,c are attributed to the Au-WSe_2 Schottky barriers, the inhomogeneous WSe_2 channel and h-BN tunneling barrier, and the adsorption impurities, that are not considered in the theoretical model. Because of the ambipolar transport property, strong light-matter interactions, the high carrier mobility, and different response mechanisms, 2D WSe_2 is an excellent candidate for realizing high-performance photodetectors.[47–49] The other experimental characterizations for gate-controlled multistate photovoltaic response of the SFG-FET are presented in Figures S4–S7 (Supporting Information).

3. Conclusion

In summary, the electrical properties and multistate photovoltaic response of a WSe_2/h-BN/graphene SFG-FET were systemically investigated both in experimental and theoretical aspects. Owing to the SFG layer and the ambipolar transport property of WSe_2, both electrons and holes can be stored in the graphene SFG layer and the device exhibits hysteresis and possesses two non-volatile memory windows. The maximum width of the memory windows is ≈60 V for $V_0 = 50$ V and the device demonstrates an excellent retention behavior. Back gate voltage dependent different junction configurations, rectification characteristics in the WSe_2 channel, and the multistate photovoltaic response are demonstrated, which combines the non-volatile memory function and the optoelectronic properties function in the SFG-FET. The capacitive and feedback tunneling coupling mechanisms between the SFG layer and the channel are incorporated into a physical model to explain the electrical properties and the multistate photovoltaic response of the SFG-FET. A quantitative relation between carrier-stored states in the SFG layer and the junction configurations in the channel is theoretically built. The simulation results are in good agreement with the experimental data. Our work is helpful for thoroughly understanding the optoelectronic properties of SFG-FETs and developing high-performance sensing-memory-processing devices.

4. Experimental Section

Heterostructure Preparation and Device Fabrication: WSe_2, h-BN, and graphite bulk crystals were purchased from the Shanghai OnWay Technology Co., Ltd. The substrate wafers (280 nm SiO_2/Si substrates) with ≈1 × 1 cm^2 sizes were cleaned by ultrasonic in acetone, isopropyl alcohol, and deionized water for 15 min and dried in N_2. Few-layer WSe_2, h-BN, and Graphene flakes were all produced with a mechanical exfoliation method from bulk crystals. Subsequently, WSe_2/h-BN/Graphene SFG-FET were prepared on a silicon wafer with 280 nm SiO_2 using dry-transfer approach under the help of an optical microscope. Then the floating-gate, drain, and source electrode patterns were defined via electron-beam lithography and lift off, followed by Pt/Au (15 nm/80 nm thickness) deposited using thermal evaporation. Finally, the device was annealed at low argon pressure of 473 K and 156 Pa for 120 min. The annealing process does not only remove impurities from the substrate surface, but also makes the 2D materials adhere more tightly to the substrate, thereby optimizing the performance of the device.

Device Characterization: The optical microscopic images of the devices were obtained by an optical microscope (OLYMPUS, BX53M). The height profiles of the van der Waals nanoflakes in these heterostructures were characterized by the atomic force microscope (Bruker, Dimension Icon with Scan Asyst). The Raman spectra were obtained by using a HR800 Raman spectrometer (French HORIBA Jobin Yvon company) with the excitation of 520-nm laser at room temperature. The Keithley 4200-SCS semiconductor analyzer was employed to characterize the electrical properties. The retention characteristic of the device was obtained by detecting the change of channel current with time (1000 s) after applying one-second-long back gate voltage pulse (40 V and −40 V). After the laser (520 nm) being applied, the photocurrents at different light intensities were obtained. The laser power was adjusted using an attenuator.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

field-effect transistor, lateral pn junction, photovoltaic response, semi-floating gate, WSe_2

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