



Non-volatile and multistate terahertz response in semi-floating-gate graphene field-effect transistors

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Abstract: Two-dimensional (2D) material photodetector based on semi-floating gate (SFG) structure is expected to achieve multiple functions of information sensing, storage, and processing in a single device. Here, we demonstrated a terahertz (THz) detector based on the graphene/h-BN/graphene SFG structure. The device exhibits an excellent memory behavior and a gate-controlled non-volatile and multistate photothermoelectric (PTE) THz response. A theoretical model is established to systematically investigate the memory and PTE response characteristics, and the numerical results are well consistent with the experimental results. Our research provides valuable insights into the complex optoelectronic behavior of 2D material Semi-Floating-Gate Graphene Field-Effect Transistors (SFG-FETs) and paves the way for the realization of multifunctional photodetectors based on SFG-FET structures.

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1. Introduction

Photodetectors capable of integrating multiple functions such as information sensing, storage, and processing hold significant potential for applications in the Internet of Things (IoT) and edge computing. Combining floating-gate non-volatile memory with photodetection is one of the important schemes to achieve such devices. 2D materials, including graphene and transition metal dichalcogenides (TMDCs), are widely used in high-performance photodetectors and floating-gate (FG) FETs [1–6], owing to their atomic-level thickness, lack of surface dangling bonds, and the ability to construct various van der Waals (vdW) heterostructures. VdW-stacked FG memory devices based on 2D materials have made remarkable progress in recent years. Furthermore changing from a full FG to a SFG to achieve gate-voltage controllable non-volatile lateral pn junctions within the channel has created various possibilities for the realization of gate-controlled, non-volatile, and multistate optoelectronic devices [7–13]. The use of SFG enables gate voltage control within the channel for a non-volatile lateral pn junction. For example, by altering the polarity and concentration of charge carrier in the SFG, different junction states can be achieved in the MoTe₂ channel, and logical functions can be realized through the optoelectronic modulation of the charge carrier concentration and polarity within the SFG [14,15]. The integration of flash memory, ultra-fast programming, and computation in 2D material floating-gate FETs reduces power consumption and time delay in memory access [16–18]. By optimizing the barrier height and gate coupling ratio, ultrafast programming and erasing speeds of 20 ns have been achieved [19]. Similarly, the stacking of a variety of vdW heterostructures has also

shown fascinating optoelectronic characteristics. In a $\text{ReS}_2/\text{h-BN}/\text{multi-layer graphene (MLG)}$ SFG device, electrical and optical tunable multi-level and non-volatile storage behavior was demonstrated [20]. An $\text{InSe}/\text{h-BN}/\text{MLG}$ FG memory device with high-quality interfaces has achieved a storage time of 10 years, ultra-fast programming and erasing speeds of 21 ns, and an erase/program ratio of 10^{10} . By controlling the number of applied short pulses, multi-value storage (4-bit) has been successfully realized [21]. Zhou et al demonstrated the heterogeneous integration capabilities of 2D materials to realize a non-volatile heterojunction mid-infrared photodetector for multi-state switching functions. The functions of infrared light detection, storage, and computation are integrated in the same device [22,23].

The 2D semiconductor materials, including MoS_2 , MoTe_2 , ReS_2 , and WSe_2 are commonly used in the channels of FG FETs and as photodetection materials [7,14,15,24–26]. The presence of a semiconductor bandgap significantly improves the on-off ratio, but it also limits the frequency range of the photoresponse [3,27–32]. There are no investigations on photodetectors based on SFG-FET structures with graphene as the channel material. Utilizing graphene as both the channel and SFG material is expected to enable the realization of high-speed, highly sensitive, and broadband photodetectors having multi functions including information sensing, storage, and processing in THz and long-wave infrared regions.

2. Results and discussion

2.1. Structure and working principle

Figure 1 shows the structure of the SFG-FET as well as the principle schematic diagrams for non-volatile and PTE photoresponse. As shown in Fig. 1(a), the device fabricated on a $\text{p}^+ \text{-Si}/\text{SiO}_2$ substrate, consists of a multi-layer graphene (MLG) SFG, an h-BN tunneling layer, and a few-layer graphene (FLG) channel layer. First, the FLG, h-BN, and SFG MLG are precisely transferred to a $\text{p}^+ \text{-Si}/\text{SiO}_2$ (with a SiO_2 layer thickness of 280 nm) substrate to form vdW heterostructures using standard mechanical exfoliation and polydimethylsiloxane (PDMS)-assisted dry transfer techniques. In these structures, MLG serves as the FG layer, h-BN as the tunneling barrier layer, and FLG as the channel layer. Additionally, SiO_2 and $\text{p}^+ \text{-Si}$ function as the back-gate layer and back-gate contact, respectively. The FG layer and the channel layer only partially overlap vertically, creating a SFG structure. Subsequently, Cr/Au (15 nm/80 nm) electrodes are fabricated using standard electron beam lithography (EBL), thermal evaporation, and thermal acetone lift-off processes. Finally, the devices are annealed in an Ar atmosphere at 473 °C for 120 minutes to remove adsorbed impurities on the device surface and enhance device stability. The detailed process information on the device fabrication is depicted in Fig. S1 for Supplement 1. For the MLG and FLG, turbostratic layer structures are approximated, which preserves the Dirac-type band-structures are maintained and results in a density of states (DOS) proportional to the number of layers. Figure 1(b) illustrates the energy band alignments of MLG (FLG) and h-BN at zero back-gate voltage (V_{BG}) [33]. Since the energy differences between the Dirac point of MLG (FLG) and the conduction and valence band edges of h-BN are 2.6 eV and 3.3 eV, respectively, only electron tunneling processes across the h-BN layer are considered. Figure 1(c) shows a schematic diagram of carrier distribution in the SFG-FET device when $V_{\text{BG}} > 0$ V. When a positive back-gate voltage is applied and the electric field on the h-BN floating gate exceeds the threshold electric field of the Fowler-Nordheim (F-N) tunneling, electrons in the FLG channel will tunnel into the MLG SFG layer through F-N tunneling, resulting in a negative charge accumulation in the SFG layer. As the electron concentration in the MLG SFG layer increases, the screening electric field generated by the captured electrons eventually reduces the total electric field across the h-BN layer to the threshold value of the F-N tunneling, which prevents the further increase of the electron concentration in the MLG SFG layer. At this point, the carrier concentration and type in the left FLG channel side (above the SFG) are determined by the charge concentration and type in the SFG layer and the back gate $\text{p}^+ \text{-Si}/\text{SiO}_2$ interface.

Conversely, when a large negative bias is applied to the back gate, and the electric field on the h-BN floating gate exceeds the threshold of the reverse F-N tunneling, electrons in the MLG SFG layer will tunnel into the FLG channel, and the MLG SFG layer becomes positively charged at steady state. By varying the back gate voltage, the net charge concentration within the SFG layer can be continuously adjusted. Under the combined influence of the back gate and the MLG floating gate, the electrostatic doping concentration and polarity in the left and right channels can be tuned over a wide range, forming different lateral homogeneous junction states, with typical configurations of pn and np junctions. It is worth noting that when the thickness of the h-BN tunneling layer is thick enough, direct tunneling can be neglected, and if the electric field across the h-BN layer does not induce F-N tunneling, the charge concentration in the MLG SFG layer remains unchanged, enabling non-volatile memory functionality. Our numerical calculations indicate that, depending on the polarity of the charge stored in the MLG SFG layer, a fixed value of V_{BG} can be applied to erase the captured charges in the SFG layer, with the erase value of V_{BG} being related only to the polarity of the stored charge and not to the charge concentration.

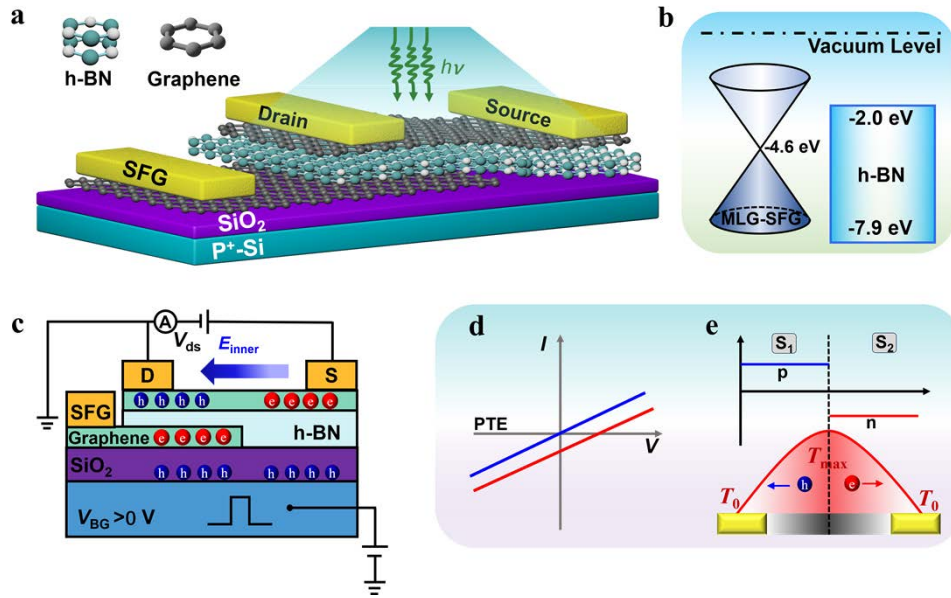


Fig. 1. The structure and working principle of the FLG/h-BN/MLG SFG-FET. a) Schematic diagram of the FLG/h-BN/MLG SFG-FET structure, where graphene serves as both the channel and FG materials, h-BN acts as the tunneling layer, Cr/Au functions as the source and drain metal electrodes, and p^+ -Si serves as the control gate. b) Energy band alignments of graphene and h-BN at $V_{BG} = 0$ V. c) The schematic diagram of gate-tunable lateral pn junction in FLG/h-BN/MLG SFG-FET When $V_{BG} > 0$ V. d) PTE I - V characteristic curves and the photoresponse principle.

When a non-volatile lateral pn junction is formed along the SFG-FET channel, zero-bias photodetection can be achieved. However, if the incident photon energy is below twice the Fermi energy (E_F), interband transitions are forbidden due to Pauli blocking, and the photovoltaic response is prohibited. In this case, the photoresponse is primarily attributed to the PTE effect. As shown in Fig. 1(d)-(e), since the thermal conductivity of the two metal electrodes is significantly higher than that of graphene [34,35], the light absorption of the MLG channel results in a temperature distribution where the middle region is hotter and the temperature gradually decreases toward the metal electrodes. Holes and electrons diffuse from the hot region to the cold regions along the temperature gradient, generating a Seebeck electromotive force V_{PTE} , which is

expressed by

$$V_{\text{PTE}} = (T_{\text{max}} - T_0) \times (S_1 - S_2) \quad (1)$$

where T_{max} represents the maximum electron temperature, T_0 is the room temperature, S_1 and S_2 are the Seebeck coefficients of p-type and n-type regions of the MLG channel, respectively. Due to the opposite signs of the Seebeck coefficients in the p-type and n-type regions, the PTE responses reinforce each other for the lateral pn junction. Because the intraband absorption is not limited by the bandgap and Pauli blocking, the SFG-FET device can achieve broadband PTE photodetection.

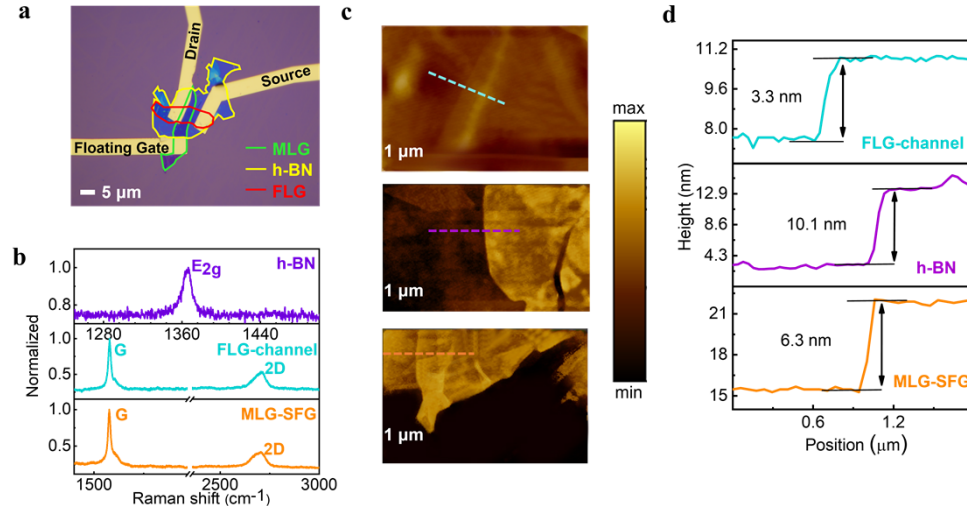


Fig. 2. Structural characterization of the FLG/h-BN/MLG SFG-FET. a) Optical micrograph of the FLG/h-BN/MLG SFG-FET structure on a $\text{SiO}_2/\text{p}^+\text{-Si}$ substrate, with different materials highlighted by solid red lines (FLG channel), yellow (h-BN), and green (MLG SFG layer). b) Raman spectra of h-BN, MLG, and FLG. c) and d) AFM images of the FLG/h-BN/MLG SFG-FET and thicknesses of different 2D materials, respectively.

2.2. Structural characterization

Figure 2(a) shows an optical micrograph of the SFG-FET device, where FLG, h-BN, and MLG are marked by solid red, yellow, and green lines, respectively. The MLG serves as the SFG, ensuring that the device maintains excellent retention performance even under high charge trapping concentration due to the high DOS [36]. The Raman spectra of h-BN, MLG, and FLG were measured by a 520-nm laser excitation. There is no layer-number-dependent difference between the MLG and the FLG. The G peak of graphene can be clearly observed at 1580 cm^{-1} , while the 2D peak is observed at 2750 cm^{-1} . The G peak is significantly higher than the 2D peak, indicating that the graphene is multilayered. The Raman peak of h-BN is located at 1362 cm^{-1} , corresponding to the E_2g mode. The above typical characteristic peaks indicate that the mechanically exfoliated materials have high quality. The morphology of the FLG/h-BN/MLG SFG-FET was characterized using atomic force microscopy (AFM), and the results are shown in Fig. 2(c). The AFM image clearly shows that the SFG-FET flake is flat and wrinkle free, with no obvious impurities between the layers. This indicates that the 20 and 30. Here, the choice of h-BN tunneling layer thickness ensures that the device can achieve F-N tunneling within a $\pm 50\text{ V}$ back-gate voltage range while simultaneously limiting the direct electron tunneling process [37]. If the h-BN tunneling barrier is too thin ($<7\text{ nm}$), the probability of direct tunneling increases, which will greatly reduce the retention performance. On the other hand, if the h-BN is too thick

(18-30 nm), it will decrease the F-N tunneling efficiency, leading to slower programming speed and higher F-N tunneling threshold voltages. Therefore, the most suitable tunneling thickness is approximately 10 nm [36].

2.3. Memory behavior and numerical results

We first measured the transport properties of the MLG/h-BN/FLG SFG-FET at room temperature. Fig. S2 for Supplement 1 shows that under zero back-gate bias and $V_{ds} = 0.02$ V, the channel current reaches approximately 15 μ A. The linear and symmetric output current-voltage curve indicates good ohmic contacts between the FLG and the Cr/Au interfaces [38]. Figure 3(a) presents the memory characteristic curve (I_{ds} - V_{BG}) of the MLG/h-BN/FLG SFG-FET, where V_{ds} was fixed to 0.01 V, and V_{BG} was swept at a rate of 0.2 V/s to ensure that the source-drain current (I_{ds}) reaches a stable value at each V_{BG} point. As V_{BG} is swept from -40 V to 40 V, the channel current first decreases to the extremum point at a gate voltage of -10 V, and then gradually increases, indicating that the initial FLG channel is n-type doped, and the output characteristic curve exhibits a typical n-type dominated bipolar FET behavior. Electrostatic doping of electrons and holes in the channel can be achieved by changing V_{BG} . As V_{BG} gradually

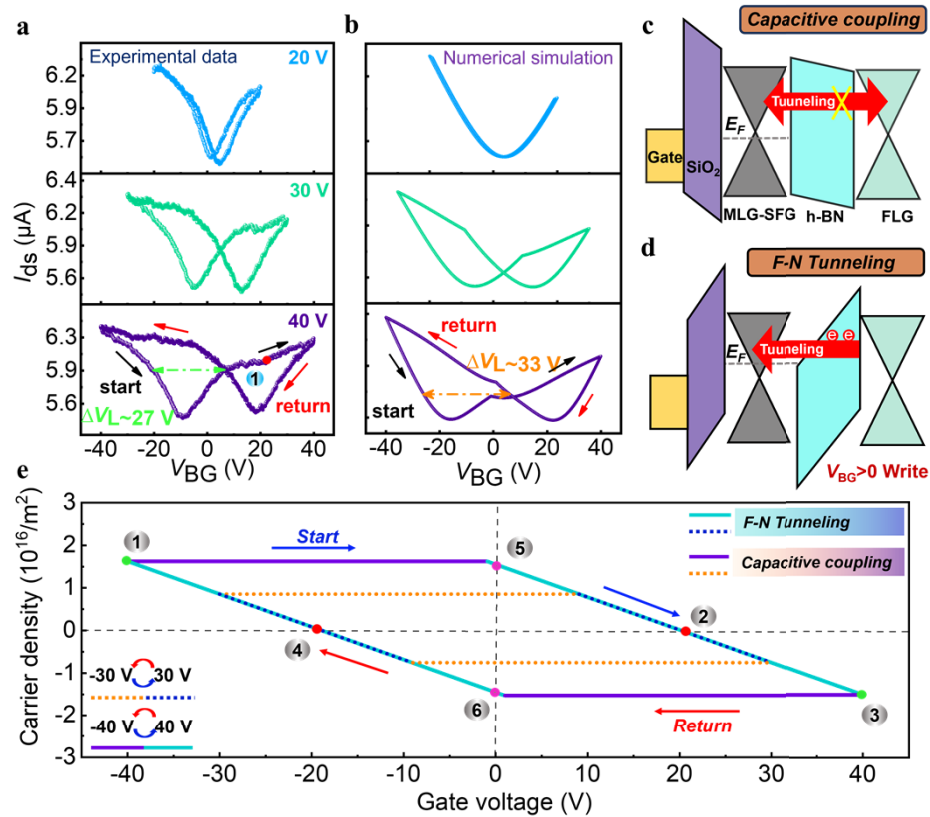


Fig. 3. Memory behavior and numerical results of the FLG/h-BN/MLG SFG-FET. a), Round-trip transfer characteristic curves under different back gate voltage conditions (V_{BG} in ± 20 V, ± 30 V, ± 40 V regions), with a fixed $V_{ds} = 0.01$ V. The sweeping speed of V_{BG} is 0.2 V/s; b), Numerical results of round-trip transfer characteristic curves; c), the SFG-FET in the capacitive coupling state; d), the SFG-FET in the feedback F-N tunneling coupling state. e), Numerical results of the net carrier concentration in the SFG layer with respect to V_{BG} (V_{BG} from -30 V to 30 V and -40 V to 40 V round-trip sweepings).

shifts positively and sweeps back to +20 V, the extremum point appears again. The SFG-FET exhibits a double extremum point type transfer characteristic curve with a significant hysteresis behavior [39]. The crossing hysteresis presents a counterclockwise non-volatile butterfly-shaped memory window (ΔV). Since MLG has a higher DOS than monolayer graphene, Fermi level has a smaller range of variation with the change in stored charge concentration, which is conducive to increasing the range of stored charge concentration changes. The large hysteresis window observed in the transfer characteristic curve indicates that the device has non-volatile memory characteristics and possesses strong potential for multi-level data storage. [15] As V_{BG} increases in 10 V steps, the ΔV window of I_{ds} - V_{BG} curve grows linearly with the round-trip sweeping range of V_{BG} (Fig S3 for Supplement 1). The maximum values of the left and right memory windows (ΔV_L and ΔV_R) are 27.5 V and 27.9 V, respectively. The relationship between the stored carrier concentration in the FG and the memory window width in the SFG-FET is given by $n_{2D} = \Delta V_{BG} \times C_{FG-BG}$, where $C_{FG-BG} = \epsilon_0 \epsilon_b / d_b$ is the back-gate SiO₂ capacitance, with ϵ_0 , ϵ_b , and d_b being the vacuum permittivity, the relative permittivity of SiO₂ (~3.9), and the thickness of SiO₂ (280 nm), respectively. This results in a storage electron concentration on the order of $\sim 2.1 \times 10^{16} \text{ cm}^{-2}$, a value comparable to other reported FG-FETs based on 2D materials. This indicates that the MLG SFG layer provides a broad storage range and good cycling stability for memory devices. The width of the memory window increases with the increase of the sweeping range of V_{BG} , indicating a significant accumulation of charge in the MLG SFG layer. When the round-trip sweeping of VBG (-40 V ~ 40 V) is repeated for about 20 cycles, the memory window (ΔV) decreases gradually from 27 V to 22 V, which maybe originate from the oxidation-induced degradation of the metal-graphene interfaces. This also indicates that the memory device exhibits a high degree of tunability and controllable data storage levels. Additionally, several other SFG-FETs with similar structures were fabricated, as shown in Fig.S4 for supporting content. Similar memory behaviors were observed, demonstrating the good reproducibility of our SFG-FETs. When V_{BG} is swept from -40 V to 40 V with $V_{ds}=0.01$ V, and the SFG layer is grounded, as shown in Fig. S5 for Supplement 1, the hysteresis window almost disappears in the round-trip transfer curve, which indicates that the memory characteristics of the device originate from the charge capture and storage of the SFG layer. To further investigate the large non-volatile hysteresis window in the transfer characteristic curve, a theoretical model was built to study the memory properties of the SFG-FET. In the model, the capacitive coupling and the feedback F-N tunneling coupling (Fig. 3(d)) play key roles on the non-volatile memory properties [40,41]. The detailed information about the model is provided in the Supplement 1, and the parameters used in the numerical calculations are listed in Table S1 for Supplement 1. The numerical results shown in Fig. 3(b) are in good agreement with the experiments (Fig. 3(a)), which confirms that the existence of the memory window in SFG-FETs depends on two different coupling states: capacitive coupling and the feedback F-N tunneling coupling between the SFG and the FLG channel [42]. Under the capacitive coupling, since the electric field on the h-BN barrier is below the threshold electric field of F-N tunneling, carriers cannot directly tunnel through the h-BN barrier, as shown in Fig. 3(c), and the carrier concentration in the SFG layer remains unchanged. When the back-gate voltage is changed such that the electric field on the h-BN tunneling barrier exceeds the F-N tunneling threshold, electrons will tunnel from the channel to the SFG layer or vice versa. Simultaneously, a screening electric field opposite to the applied electric field is formed. When a steady state is reached, the superposition electric field equals the F-N tunneling threshold field, thereby closing the F-N tunneling process. According to literature [42], we refer to this phenomenon as feedback F-N tunneling coupling (Fig. 3(d)). Due to charge trapping and storage within the SFG layer, the carrier concentration and polarity of electrostatic doping on the left side of the channel (Fig. 1(a), drain) are determined jointly by the back gate voltage and the captured carrier concentration in SFG, while the right side of

the channel (Fig. 1(a), source end) is determined solely by the back gate voltage. Consequently, different lateral homogeneous junctions are formed in the FLG channel.

To gain a clearer understanding of the non-volatile memory and photoresponse behaviors of the device, the net charge concentration within the SFG layer as a function of the round-trip sweeping of V_{BG} was numerically calculated and the results are presented in Fig. 3(e). At $V_{BG} = -40$ V, the applied electric field on the h-BN barrier is larger than the negative threshold field of F-N tunneling and its direction is from the FLG channel to the SFG layer. The applied electric field leads to the F-N tunneling of electrons from the SFG layer to the FLG channel. The direction of resultant screening electric field points from the SFG layer to the FLG channel, which leads to the reduction of the superimposed electric field on the h-BN barrier. Finally, a steady state is reached, in which the electron F-N tunneling stops and the superimposed electric field on the h-BN barrier is pinned at the negative threshold field of F-N tunneling. When V_{BG} is swept from -40 V to -1 V (1-2 section in Fig. 3(e)), the total electric field gradually decreases to zero, and then its direction is reverse and increases to the positive threshold value of F-N tunneling. During this period, the F-N tunneling channel is closed, the device in a capacitive coupling state, and the charge concentration in the SFG layer remains constant. When V_{BG} is swept from -1 V to 40 V (2-4 section in Fig. 3(e)), the superimposed electric field across the h-BN barrier is pinned at the positive threshold value for F-N tunneling, enabling electrons to tunnel from the FLG channel to the SFG layer. The charge concentration in the SFG layer varies linearly with V_{BG} , and the device operates in a feedback F-N tunneling state. When V_{BG} is swept in reverse from 40 V to -40 V, the device transitions successively to capacitive coupling and feedback F-N tunneling states, with the microscopic processes being similar to the case of forward sweeping. It is worth noting that once the device structure is determined, the change in excess charge concentration in the SFG layer during the feedback F-N tunneling periods follows two straight lines with respect to V_{BG} , and the intersections with the x -axis represents the excess charge erase points in the SFG layer. When the stored charge is positive (negative), the erase value of V_{BG} is approximately 20 (-20) V. It can also be observed that when the programming value of V_{BG} is excessively high (e.g., -40 V or 40 V in Fig. 3), after the gate voltage is removed, as shown at points 5 and 6 in Fig. 3(e), charge leakage will occur. The numerical calculations do not account for the in-plane non-uniformity of each layer and approximated the F-N tunneling probability as a step function that jumps from 0 to 1 at the threshold field. These approximations and simplifications may introduce some deviations from the real situation, but the numerical results indicate that our model can describe the device operation process with a relatively high degree of accuracy.

2.4. Response of the SFG-FET and experimental results

In Fig. 4, the THz PTE response characteristics of the SFG-FET are presented. Figure 4(a) shows the PTE photocurrent of the SFG-FET at room temperature and zero bias voltage ($V_{ds} = 0$ V) across the frequency range of 70 to 110 GHz, with an incident power density of 1 mW/cm^2 , and the peak response frequency is observed at 90 GHz. The peak photoresponse at 90 GHz may be attributed to the antenna enhancement effect of the electrodes. For graphene, there are two THz absorption processes, the intraband and the interband transitions. Therefore, the SFG-FET detector is broadband. For uniform illumination, an asymmetric device structure is necessary for a PTE response. In the SFG-FET, the asymmetry origins from the different carrier concentrations in the left and right regions of the FLG channel. Due to the absence of a coupling structure and the deep-subwavelength dimension of the device, the THz absorption efficiency is very low, resulting in a low PTE responsivity of approximately $1.2 \times 10^3 \text{ A/W}$. The power-dependent photocurrent is shown in Fig. S7 with the incident power from 1 mW to 10 mW and the frequency of 16.7 GHz. The linear photocurrent response shows that the device has a wide dynamic range. For improving the detection performance of the SFG-FET device, THz couplers, such as antennas, plasmonic structures and microcavities, can be introduced.

Figure 4(b) displays the photocurrent waveform under illumination by square-wave-modulated 90 GHz radiation, indicating that the device exhibits a relatively fast response speed due to the hot electron PTE effect, with arising response time of 72 μs and a falling response time of 100 μs . Due to the hot carrier effect of FLG channel, the intrinsic PTE response is very fast [43,44], the slow rise/fall times shown in Fig. 4(b) are limited by the RC time of the measurement circuit. In addition, the SFG-FET exhibits a polarization-dependent PTE response, demonstrating sensitivity to the orientation of the incident radiation. When the polarization direction of the THz electric field is aligned with the FLG channel, the photocurrent is enhanced to about twice of that for

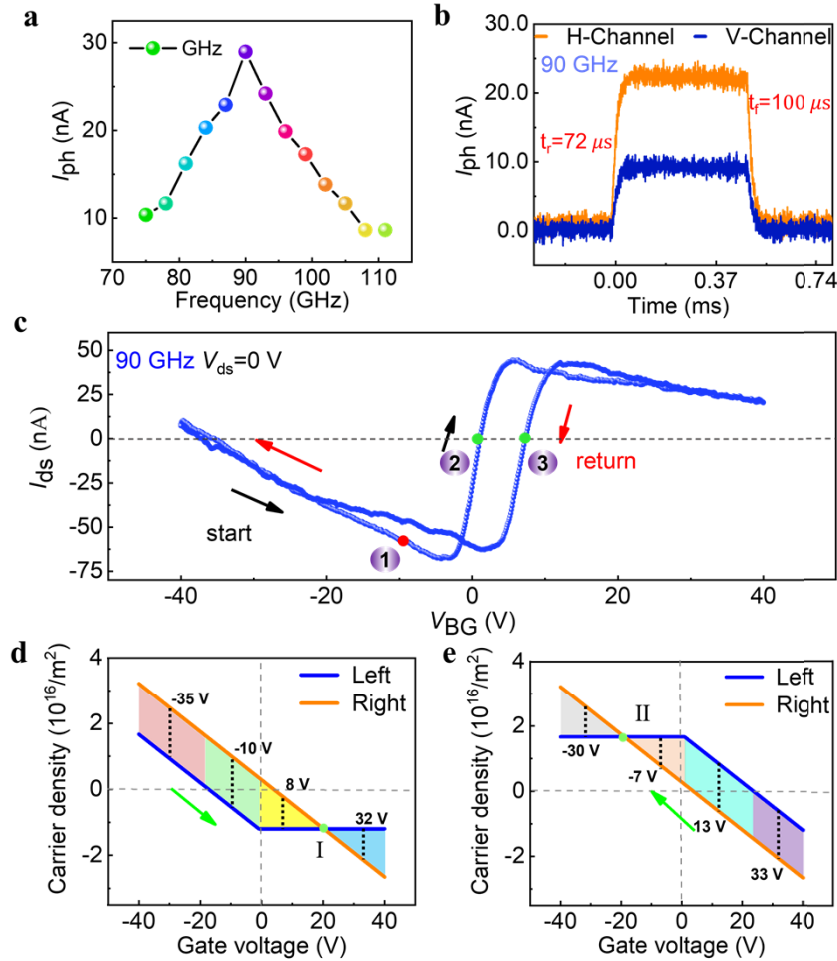


Fig. 4. THz PTE response of the SFG-FET with respect to V_{BG} and the numerical results of carrier concentrations of left and right region of FLG channel. a), Wavelength-dependent photocurrents of the SFG-FET at $V_{ds} = 0$ V and $V_{BG} = 0$ V (70 GHz - 110 GHz); b), PTE zero-bias photocurrent waveforms at 90 GHz with the polarizations of the normally incident THz field aligned parallel and perpendicular to the FLG channel (Respectively denoted as H and V); c), Zero-bias THz (90 GHz) photocurrents with respect to V_{BG} round-trip sweeping in the range of -40 V to 40 V. d) Numerical results of carrier concentrations in the left and right regions of the FLG channel with respect to V_{BG} forward sweeping in the range of -40 V to 40 V. e) Numerical results of carrier concentrations in the left and right regions of the FLG channel with respect to V_{BG} backward sweeping in the range of -40 V to 40 V.

the case of polarization perpendicular to the channel, indicating that the antenna effect of the metal electrodes causes a localized enhancement of the electric field. Because the Seebeck coefficient of graphene depends on the carrier concentration and polarity [45], we measured the PTE photocurrent of the device at zero bias and 90 GHz illumination with V_{BG} round-trip sweeping in the range of -40 V to 40 V, and the results are shown in Fig. 4(c). It was found that the PTE response of the SFG-FET exhibits a dependence on gate voltage. This is because the gate voltage can adjust the carrier concentration in the left and right region of the FLG channel through capacitive coupling and feedback F-N tunneling coupling, thereby inducing variations in the Seebeck coefficient. For global and uniform THz illumination, due to the large thermal capacity and thermal conductivity of the source and drain electrodes, the temperature change caused by THz irradiation at the graphene-metal contacts is minimal, while in the central region of the FLG channel there will be a distinct temperature rise. At this time, since the V_{BG} -controlled lateral homogeneous junction is formed in the channel, a V_{BG} -dependent PTE response is expected. Additionally, it can be observed that the zero-bias PTE response of the device exhibits hysteresis behavior with round-trip sweeping of V_{BG} , further demonstrating the influence of the lateral homogeneous junctions induced by the SFG on the THz response. To better understand the zero-bias PTE response variation with V_{BG} as shown in Fig. 4(c), we numerically calculated the carrier concentrations in the left and right regions of the FLG channel (Fig. 4(d) and 4(e)). During the round-trip sweeping of V_{BG} , various lateral junction configurations are formed within the SFG-FET channel. When V_{BG} is swept from -40 V to -1 V, the SFG-FET operates in a capacitive coupling state. In this state, the left region of the FLG channel exhibits a reduced hole concentration, while the right region channel maintains a higher hole concentration due to the lack of influence from the SFG, resulting in a lateral pp^+ junction configuration. As V_{BG} continues to sweep forward, the hole concentration decreases to zero, and the dominant carrier type transitions from holes to electrons, causing the junction configuration to change from pp^+ to np (e.g., at $V_{BG} = -10$ V). At this point, the device nearly reaches the maximum negative zero-bias photocurrent (near point 1 in Fig. 4(c)). As V_{BG} further sweeps forward, the hole concentration on the right region of the FLG channel decreases, leading to a slight decrease in PTE response. At this point, the dominant carriers throughout the FLG channel become electrons, forming an n^+n junction. Within this region, the capacitive coupling state transitions to the feedback F-N tunneling state, during which the photocurrent changes rapidly. For backward sweeping of V_{BG} , as shown in Fig. 4(c), a similar trend is observed for the V_{BG} dependent PTE response. Due to the non-volatile memory effect of the SFG-FET, the photocurrent curve exhibits a positive shift during backward V_{BG} sweeping. Point II of Fig. 4(e) corresponds to the uniform carrier concentration in the FLG channel, at which the PTE response approaches to zero. As shown in Fig. 4(c), there are two zero PTE response points (points 1 and 2). However, there are large discrepancies of V_{BG} values, at which the PTE responses reach to zero. The discrepancies between the numerical results and the experimental data are primarily attributed to factors not considered in the theoretical model, such as the doping effect near the Au-graphene interfaces, the non-uniform FLG channel and the h-BN tunneling barrier, as well as impurities adsorbed.

3. Conclusions

In summary, a fully 2D material-based FLG/h-BN/MLG SFG-FET was novelly designed. The electrical characteristics and multistate THz PTE response were systematically investigated through both experimental and theoretical approaches. The novel 2D material-based non-volatile memory device structure exhibits unattainable characteristics, compared with the traditional 3D materials. The bipolar graphene material, regulated by gate voltage, enables multiple state configurations in the channel layer, such as pn junctions, while the MLG-SFG layer can store electrons and holes, resulting in significant hysteresis characteristics with a maximum memory window of ≈ 27 V. By combining numerical simulation, we provide a comprehensive explanation

of the carrier dynamic in the device under capacitive coupling and feedback F-N tunneling coupling states, enabling gate voltage-dependent programming and erasing operations. Above results demonstrate a novel integration approach and the excellent memorise characteristic based on the SFG-FET structure utilizing all 2D materials, laying the foundation for the development of new non-volatile THz and infrared optoelectronic devices with logical control capabilities.

4. Experimental section

Heterostructure Preparation and Device Fabrication: Substrates with dimensions of approximately $1 \times 1 \text{ cm}^2$ (280 nm, SiO₂/Si) were ultrasonically cleaned for 15 minutes in acetone, isopropanol, and deionized water, and then dried in N₂. Few-layer graphene, h-BN, and graphene flakes were prepared by mechanical exfoliation from bulk crystals (graphene, h-BN, and other crystals were purchased from Shanghai OnWay Technology Co., Ltd.). Subsequently, under the assistance of an optical microscope, a dry transfer method was used to fabricate FLG/h-BN/MLG SFG-FETs on silicon wafers containing 280 nm SiO₂. Next, polymethyl methacrylate (PMMA) was spin-coated and electron beam lithography (EBL) was used to define the floating gate, drain, and source electrodes, followed by thermal evaporation to deposit Cr/Au (15 nm/85 nm thickness). Finally, the devices were completed using a standard lift-off process.

Device Characterization: The optical microscopic images of the devices were obtained by an optical microscope (OLYMPUS, BX41 M). The height profiles of the van der Waals nanoflakes in these heterostructures were characterized by the atomic force microscope (Bruker, Dimension Icon with Scan Asyst). The Raman spectra were obtained by using a HR800 Raman spectrometer (French HORIBA Jobin Yvon company) with the excitation of 520-nm laser at room temperature. The Keithley 4200-SCS semiconductor analyzer was employed to characterize the electrical properties. After applying light of different frequencies using a microwave source, the optoelectronic properties of the device were obtained.

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Data availability. Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

Supplemental document. See [Supplement 1](#) for supporting content.

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